ic application of the month

XR-2208 Operational Multiplier

GENERAL DESCRIPTION

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing application. As shown in the functional block diagram, for maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected, with a minimum number of external components, to perform arithmetic computation, such as multiplication, division, square root extraction. The operational amplifier can also function as a preamplifier for low-level input signals, or as a post detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/buffer amplifier combination extends the small signal 3-dB bandwidth to 8 MHz and the transconductance bandwidth to 100 MHz.

The XR-2208 operates over a wide range of supply voltages, ±4.5V to ±16V. Current and voltage levels are internally regulated to provide excellent power supply rejection and temperature stability. The XR-2208 operates over a 0°C to 75°C temperature range. The XR-2208M is specified for operation over the military temperature range of −55°C to +125°C.

FEATURES

Maximum Versatility
- Independent Multiplier, Op-Amp, and Buffer

Excellent Linearity (0.3% typ.)

Wide Bandwidth
- 3 dB B.W. – 8 MHz typ.
- 3° Phase Shift B.W. – 1.2 MHz typ.
- Transconductance B.W. – 100 MHz typ.

Simplified Offset Adjustments

Wide Supply Voltage Range (±4.5V to ±16V)

APPLICATIONS

Analog Computation
- Multiplication
- Division
- Squaring
- Square Root

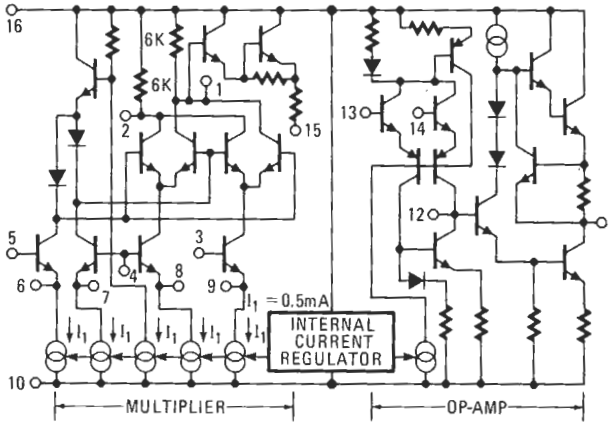
Signal Processing
- AM Generation
- Frequency Doubling
- Frequency Translation
- Synchronous AM Detection
- Triangle-to-Sinewave Converter
- AGC Amplifier
- Phase Detector

Phase-Locked Loop (PLL) Applications
- Motor Speed Control
- Precision PLL
- Carrier Detection
- Phase-Locked AM Demodulation

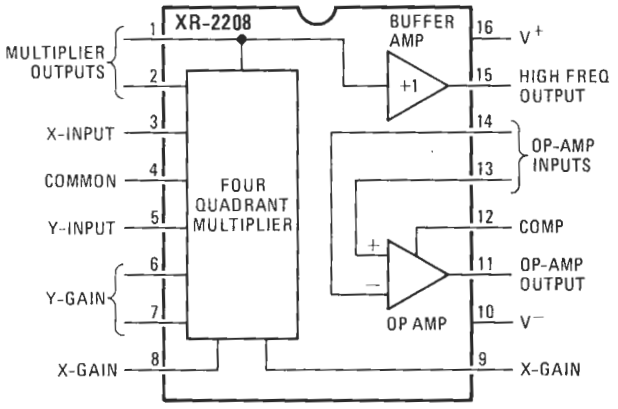
ABSOLUTE MAXIMUM RATINGS

Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mW/°C
Plastic Package	625 mW
Derate above +25°C	5.0 mW/°C
Power Supply V^+	+18 Volts
V^-	−18 Volts
Storage Temperature Range	−65°C to +150°C

SIMPLIFIED SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



EXAR INTEGRATED SYSTEM, INC.
750 Palomar Ave., P.O. Box 62229, Sunnyvale, CA 94088

AVAILABLE TYPES

Part Number	Package	Temperature Range
XR-2208M	Ceramic	−55°C to +125°C
XR-2208N	Ceramic	0°C to +75°C
XR-2208P	Plastic	0°C to +75°C
XR-2208CN	Ceramic	0°C to +75°C
XR-2208CP	Plastic	0°C to +75°C

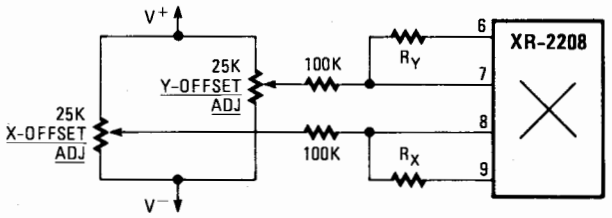


FIG. 1-OFFSET ADJUSTMENT

DESCRIPTION OF CIRCUIT CONTROLS

MULTIPLIER INPUTS (PINS 3, 4, AND 5)

The X- and Y-inputs to the multiplier are applied to pins 3 and 5 respectively. The third input (pin 4) is common to both X- and Y-portions of the multiplier, and in most applications serves as a "reference" or ground terminal. The typical bias current at the multiplier inputs is 3 μA for the X- and Y-inputs and 6 μA for the "common" terminal. In circuit applications such as "synchronous AM detection" or "frequency doubling" where the same input signal is applied to both X- and Y-inputs, pin 4 can be used as the input terminal since it is common to both X- and Y-sections of the multiplier.

MULTIPLIER OUTPUTS (PINS 1 AND 2)

The differential output voltage, V_o, across these terminals is proportional to the linear product of voltages V_x and V_y applied to the inputs. V_o can be expressed as:

$$V_o \approx \left(\frac{25}{R_x R_y}\right)\left(V_x V_y\right)$$

where all voltages are in volts and the resistors are in kΩ. R_x and R_y are the gain control resistors for X- and Y-sections of the multiplier.

The common-mode DC potential at the multiplier outputs is approximately 3 volts below the positive supply. One of the multiplier outputs (pin 1) is internally connected to the unity-gain buffer amplifier input for high frequency applications.

In most analog computation operations, such as multiplication, division, etc., pins 1 and 2 are DC coupled to the op-amp inputs (pins 13 and 14). The final output, V_z, is then obtained from the op-amp output at pin 11, as shown in Fig. 2.

X AND Y GAIN ADJUST (PINS 6, 7, 8, AND 9)

The gains of the X- and Y-sections of the multiplier are inversely proportional to resistors R_x and R_y connected across the respective gain terminals. The multiplier conversion gain, K_m, can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y} \quad (\text{volts})^{-1}$$

where R_x and R_y are in kΩ.

X- AND Y-OFFSET ADJUST (PINS 7 AND 8)

Two of the gain-control terminals, pins 7 and 8, are also used for adjusting X- and Y-offsets. Fig. 1 shows the typical adjustment circuitry which can be connected to these pins to null-out input offsets.

OP-AMP INPUTS (PINS 13 AND 14)

Pin 13 is the noninverting and pin 14 the inverting inputs for the op-amp section. In most multiplier applications, these terminals are connected to the multiplier outputs (pins 1 and 2). Note: When the op-amp section is not used, these terminals should be grounded.

OP-AMP COMPENSATION (PIN 12)

The op-amp section can be compensated for unconditional stability with a 20 pF capacitor connected between pin 12 and pin 11. For op-amp voltage gains greater than unity, this compensation capacitance can be reduced to improve slew rate and small signal bandwidth.

OP-AMP OUTPUT (PIN 11)

This terminal serves as the output for the op-amp section. It is internally protected against accidental short circuit conditions, and can sink or source 10 mA of current into a resistive load. In most multiplier applications, pin 11 is the actual XR-2208 output, with the op-amp inputs being connected to the multiplier outputs.

BUFFER AMPLIFIER OUTPUT (PIN 15)

The buffer amp is internally connected to the multiplier section. The buffer amp has unity voltage gain, and provides a low-impedance output at pin 15 for the multiplier section. The buffer amp is particularly useful for high frequency operation since it minimizes the capacitive loading effects at the multiplier outputs.

The buffer amplifier is activated by connecting a load resistor, R1, from pin 15 to ground. When it is not used, pin 15 can be left open circuited. However, since the buffer amplifier output is a low-impedance point, reasonable care should be taken to avoid burnout due to accidental short circuits. The maximum DC current drawn from pin 15 should be limited to 10 mA. The DC voltage at pin 15 is typically 4.5 volts below V^+.

APPLICATIONS INFORMATION

PART I: ARITHMETIC OPERATIONS

Multiplication

For most multiplication applications, the multiplier and op-amp sections are interconnected as shown in Fig. 3 to provide a single-ended analog output with a wide dynamic range. The circuit of Fig. 2 provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K = 0.1. The trimming procedure for the circuit is as follows:

1. Apply OV to both inputs and adjust the output offset to OV using the output offset control.
2. Apply 20V P-P at 50 Hz to the X-input and OV to the Y-input. Trim the Y-offset adjust for minimum peak-to-peak output.
3. Apply 20V P-P to the Y-input and OV to the X-input. Trim the X-offset adjust for minimum peak-to-peak output.

4. Repeat step 1.
5. Apply +10V to both inputs and adjust scale factor for V_o = +10V. This step may be repeated with different amplitudes and polarities of input voltages to optimize accuracy over the entire range of input voltages, or over any specific portion of input voltage range.

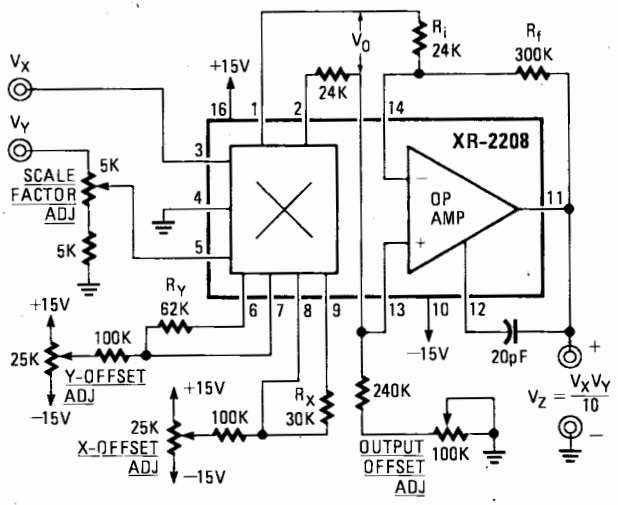


FIG. 2-MULTIPLICATION CIRCUIT

Squaring Circuit

The recommended circuit connection for squaring applications is shown in Fig. 3. This circuit is the same as the

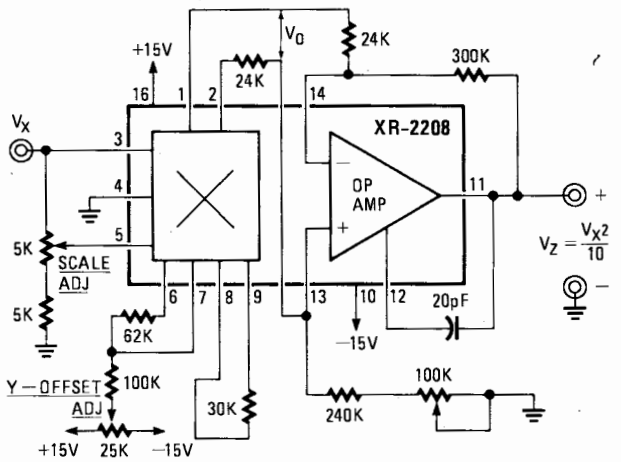


FIG. 3-SQUARING CIRCUIT

basic multiplier circuit with both inputs tied together, except only one input offset adjustment is necessary. Trimming procedure for the squaring circuit is as follows:

1. Apply 0 volts to the input and adjust the output offset to zero.
2. Apply 1.0V to the input and adjust the Y-offset until V_o = 0.10V.
3. Apply 10V to the input and adjust the scale factor until V_o = +10V.
4. Apply −10V to the input and check that V_o = +10V. If not, repeat steps 1 through 3. Some compromise may be necessary in scale factor adjustments given in steps 3 and 4.

Dividing Circuit

Recommended circuit connection for performing analog division is shown in Fig. 4. This circuit uses the multiplier

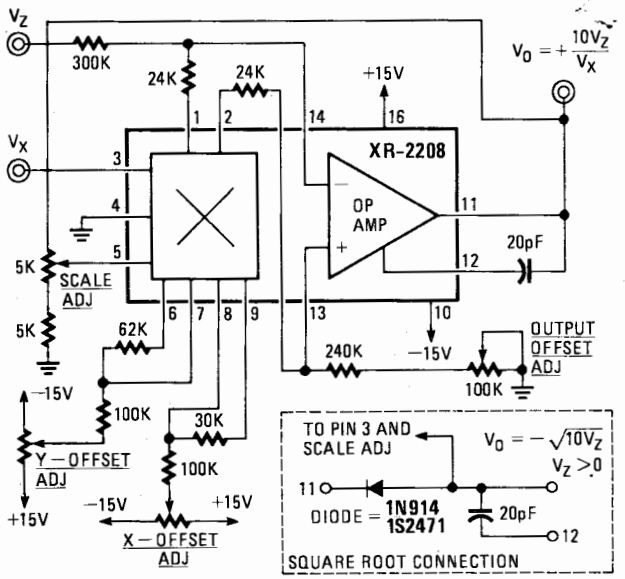


FIG. 4-DIVIDING CIRCUIT

in the feedback path of the op-amp. For the circuit shown, V_o = +10 V_Z/V_X where $V_x < 0$ and V_z can have either sign. Positive values of V_x are not allowed, causing positive feedback and latchup.

This latchup mode is nondestructive to the XR-2208, and is common to all analog division circuits. The divide circuit is trimmed as follows:

1. Apply V_z = 0 and trim the output offset adjustment for constant output voltage as V_x is varied from −1V to −10V.
2. Keeping V_z = 0, and applying V_x = −10V, trim the Y-offset adjust until V_o = 0.
3. Let $V_z = V_x$ and/or $V_z = -V_x$ and trim the X-offset adjustment for constant output voltage as V_x is varied from −1V to −10V.
4. Repeat steps 1 and 2 if step 3 required a large initial adjustment.
5. Keeping $V_z = V_x$, adjust the scale factor trim for V_o = −10V as V_x is varied from −1V to −10V.

Square Root Circuit

This is essentially the dividing circuit with the X-input tied to the output. Thus, the voltage on the Z-input is divided by the output voltage, i.e. the output is proportional to the square root of the input. A diode is included in series with the output to prevent a latchup condition which would result if V_z were allowed to go negative. The square root circuit may be trimmed as a divider by disconnecting the X-input from the output, keeping $V_z > 0$ and $V_x < 0$. The square root circuit may also be trimmed in the closed-loop mode by the following procedure:

1. Apply V_z = +0.10V and trim the output offset adjust for V_o = −0.316V.
2. Apply V_z = +0.9V and trim the X-offset adjust for V_o = −3.0V.
3. Apply V_z = +10V and trim the scale factor adjust for V_o = −10V.
4. Repeat steps 1 through 3 until desired accuracy is achieved.

PART II: SIGNAL PROCESSING

AM GENERATION

Figure 5 is the recommended circuit connection for

generating double sideband (DSB) or suppressed carrier AM signals. Modulation and carrier inputs are applied to the X- and Y-inputs respectively. The carrier level at the output can be adjusted by the DC voltage applied to pin 3. For suppressed carrier operation, the carrier feedthrough can be further reduced by using the X- and Y-offset adjustments. In this application, the unity-gain buffer amplifier section will provide a low-impedance output if desired. If the buffer amp is not used, pin 15 should be open circuited to reduce power dissipation.

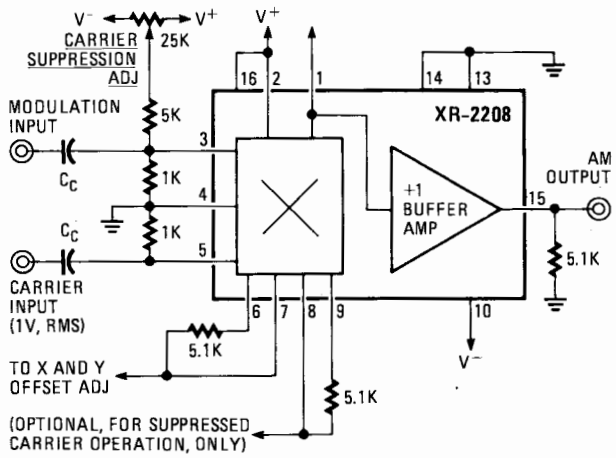


FIG. 5-AM GENERATION

Typical carrier suppression without offset adjustment is 40 dB for frequencies up to 1 MHz, and 30 dB for frequencies up to 10 MHz. For low frequency applications ($f < 10$ kHz), carrier suppression can be reduced to 60 dB by using the offset adjustment controls.

SYNCHRONOUS AM DETECTION

Figure 6 is a typical circuit connection for synchronous

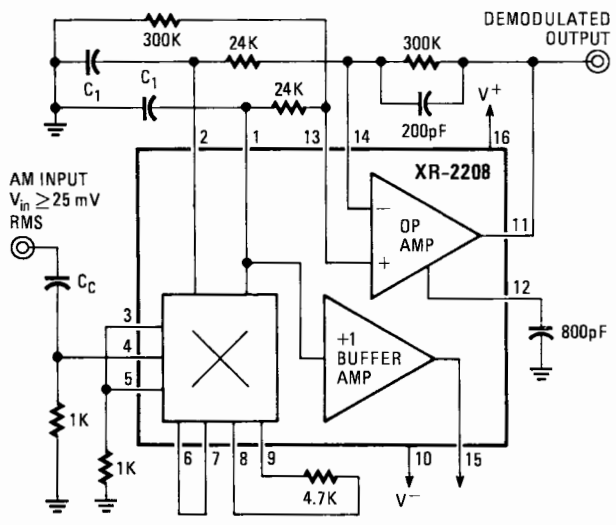


FIG. 6-SYNCHRONOUS AM DETECTOR

AM detection for carrier frequencies up to 100 MHz. The AM input signal is applied to the multiplier "common" terminal (pin 4). The Y-gain terminals are shorted, and this section of the multiplier serves as a "limiter" for input signals $\geq$ 50 mV RMS; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C1, at pins 1 and 2 are used to filter the carrier feedthrough. If desired, the op-amp section can be used as an audio pre-amplifier to increase the demodulated output amplitude.

TRIANGLE-TO-SINEWAVE CONVERSION

A triangular input can be converted into a low distortion (THD $<$1%) sinusoidol output with the XR-2208. A recommended connection for this application is shown in Fig. 7.

The triangle input signal is applied to the X-input (pin 3). The multiplier section rounds off the peaks of this input and converts it to a low distortion sinewave. For the component values shown in Fig. 7, the recommended input signal level at pin 3 is $\simeq$ 300 mV P-P in order to obtain a 2V P-P sinewave output at pin 15. This waveform can be further amplified using the op-amp section to provide high level (10V P-P), low distortion output at pin 11.

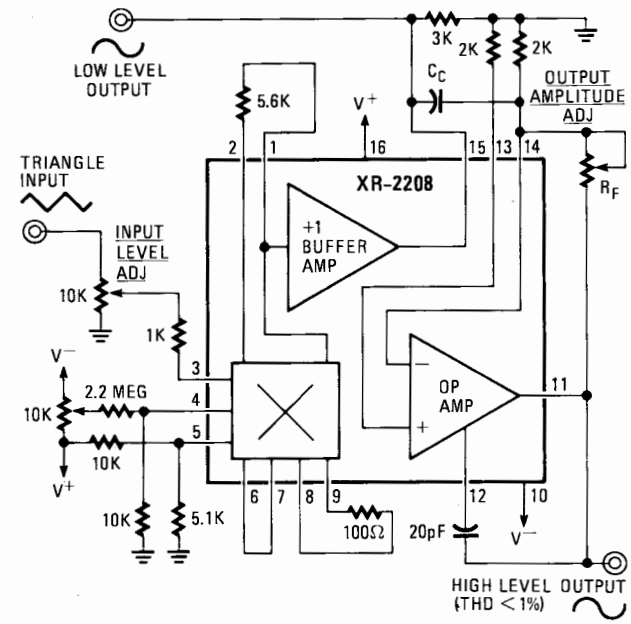


FIG. 7-TRIANGLE-TO-SINE CONVERTER

PHASE DETECTION

The multiplier section can be used as a phase detector. A recommended circuit connection is shown in Fig. 8. The

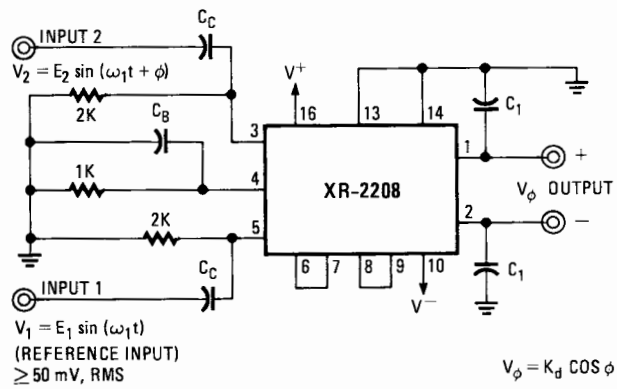


FIG. 8-PHASE-DETECTOR CIRCUIT

reference input is applied to pin 5, and the input signal whose phase is to be detected is applied to pin 3. The differential DC voltage, V_ϕ, at the multiplier outputs (pins 1 and 2) is related to the phase difference, ϕ, between the two input signals, V_1 and V_2, as:

$$V_\phi = K_d \cos\phi$$

where K_d is the phase detector conversion gain. For input signals $\geq$ 50 mV RMS, K_d is $\approx$ 2V/radian and is independent of signal amplitude. For lower input amplitudes, K_d decreases linearly with the decreasing input level. The capacitors C1 at pins 1 and 2 provide a low-pass filter with a time constant T1 = R1 C1, where R1 = 6 kΩ is the internal impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op-amp section of the XR-2208 to further amplify the output voltage, V_ϕ. The XR-2208 operational multiplier is suitable for phase detection of input frequencies up to 100 MHz.

PART III: PHASE-LOCKED LOOP APPLICATION

MOTOR SPEED CONTROL

A motor speed control where the frequency of the motor is "phase-locked" to the input reference frequency, f_r, is shown in Fig. 9. The multiplier section of the XR-2208 is

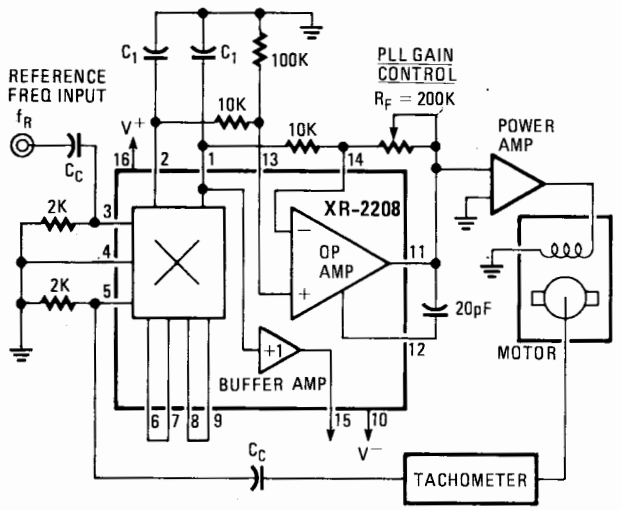


FIG. 9-MOTOR SPEED CONTROL CIRCUIT

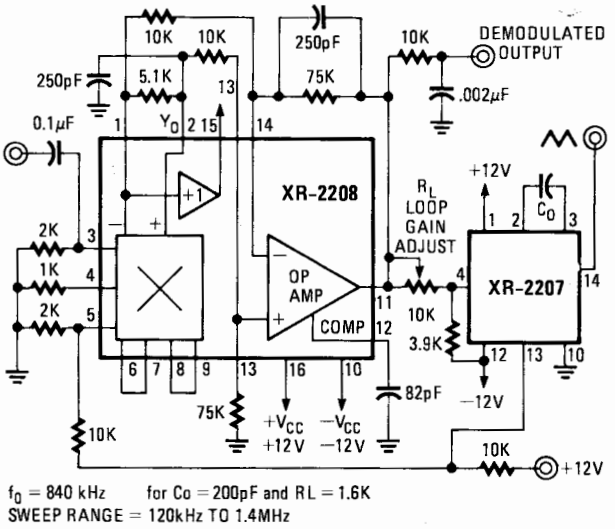
used as a phase comparator, comparing the phase of the tachometer output signal with the phase of the reference input. The resulting error voltage across pins 1 and 2 is low-pass filtered by capacitors C1 and amplified by the op-amp section. This error signal is then applied to the motor field-winding to phase-lock the motor speed to the input reference frequency.

PRECISION PLL

A precision phase-locked loop may be constructed using an XR-2207 voltage controlled oscillator and an XR-2208. (See Fig. 10.) Due to the excellent temperature stability and wide sweep range of the XR-2207 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2208 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than −30 ppm/°C.

PHASE-LOCKED AM AND CARRIER DETECTION

The XR-2208 can be used as a "quadrature detector" in conjunction with monolithic PLL circuits to perform phase-

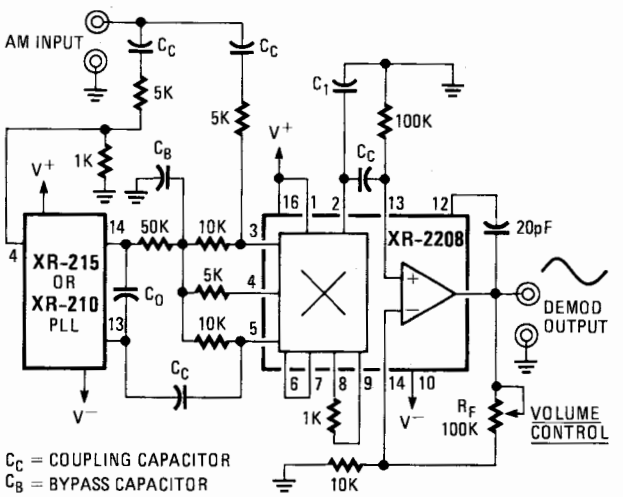


f_0 = 840 kHz for Co = 200pF and RL = 1.6K
SWEEP RANGE = 120kHz TO 1.4MHz

FIG. 10-PRECISION PLL

locked AM demodulation and for carrier-level detection. Fig. 11 shows a recommended circuit connection for such applications. The XR-210 or XR-215 monolithic PLL circuits can be adjusted to lock on the desired input AM signal and regenerate the unmodulated carrier. This carrier frequency appears across the timing capacitor, CO, of the PLL and is used as the "reference input" to the XR-2208 multiplier. The AM signal is applied simultaneously to the PLL input and to the XR-2208 multiplier input (pin 3), as shown in Fig. 11.

The demodulated signal is then low-pass filtered by capacitor C1 at the multiplier output, and can be amplified further to the desired audio level by using the op-amp section of the XR-2208.



C_C = COUPLING CAPACITOR
C_B = BYPASS CAPACITOR

FIG. 11-PHASE-LOCKED AM DEMODULATION OR CARRIER DETECTION

In the carrier detector applications, the op-amp is used as a voltage comparator and produces a "high" or "low" level logic signal at the op-amp output when the input carrier level reaches a detection threshold level set by an external potentiometer. The output from the carrier detector can then be used to enable the "logic-output" stage of the XR-210 FSK modem.

The phase-locked AM or carrier detector system of Fig. 11 shows a high degree of frequency selectivity, as determined by the monolithic phase-locked-loop "capture" bandwidth. **R-E**