Comparators and resistors form clockless a-d converter

by Adrian H. Kitai
Hamilton, Ont., Canada

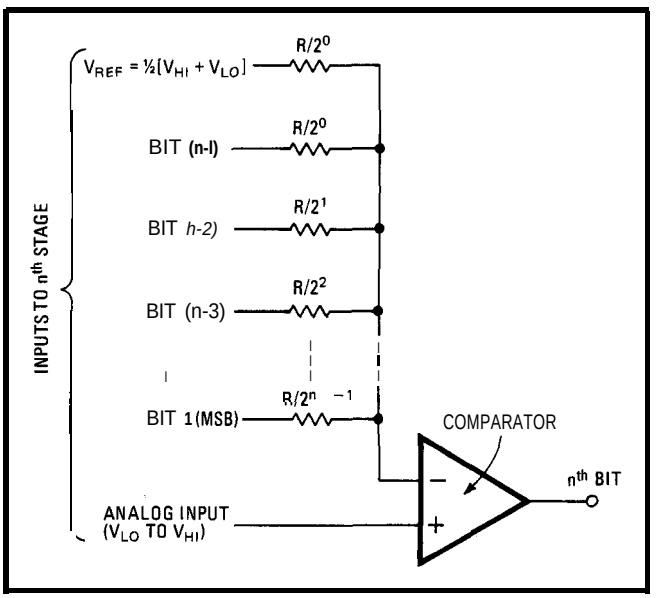
A successive-approximation analog-to-digital converter can be built out of comparators and resistors only. Conversion speed is determined by the settling time of the comparators, and no clock is needed.

The concept is illustrated in Fig. 1, which shows the n^{th} stage of a converter. The analog input voltage is compared with a voltage, the value of which is determined by the outputs of all previous stages, as well as by Vref. A resistor is connected to weight each of the previous comparator outputs, and an additional resistor is connected to Vref, which must be midway between the HI and LO levels of the comparator's output voltage. The n^{th} comparator needs n resistors, except for the first stage which needs none.

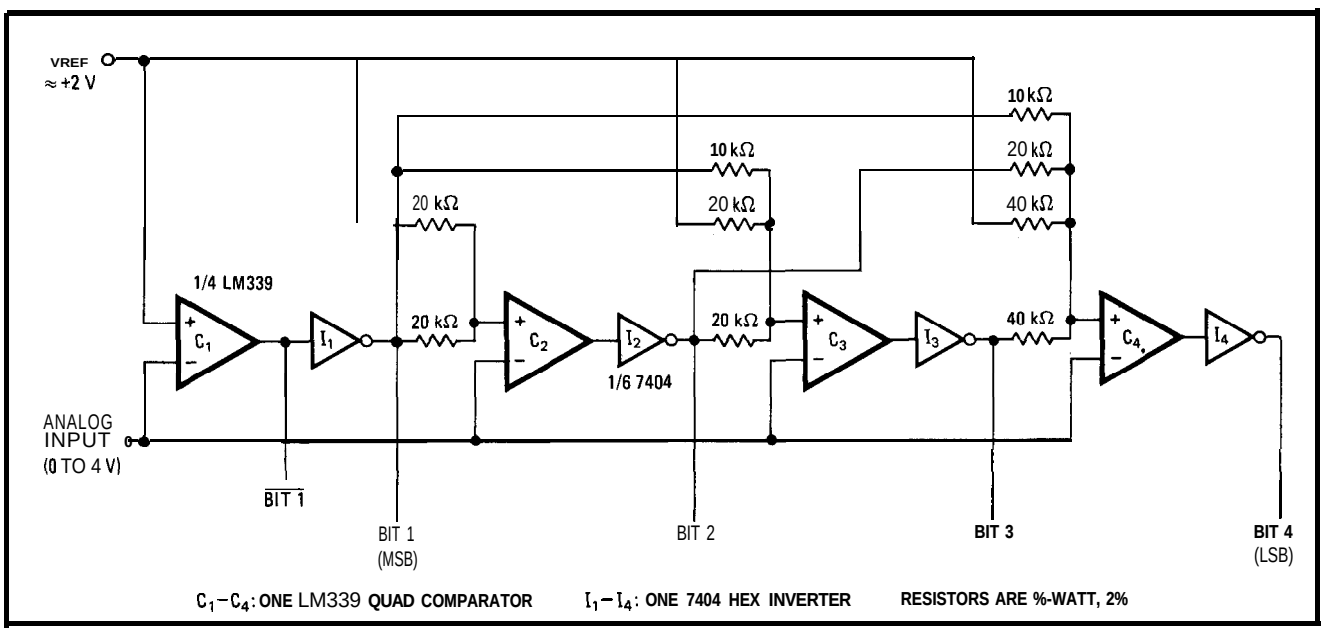
Since, however, the open-collector outputs of the comparators do not deliver voltages of sufficient precision, they are in practice followed by inverters that clamp the voltages. To compensate for this inversion of the comparator output, the input connections to the comparators are the reverse of those shown in Fig. 1; i.e., the analog input signal is connected to the inverting inputs instead of to the noninverting inputs.

Figure 2 shows a practical 4-bit circuit that uses only two inexpensive integrated circuits. This circuit is useful for applications such as driving a display of 16 light-emitting diodes. Comparator C_1 has its positive input tied to Vref. When an analog input lying between ground and 2Vref (near +4 volts) is applied to the negative input, the output of inverter I, is the first bit. This output is used to establish the switching level for C_2, which is either $\frac{1}{2} V_{ref}$ or $\frac{3}{2} V_{ref}$ depending on whether I_1's output is LO or HI. In the same way, the remaining comparators provide bits 3 and 4.

To understand the circuit's operation, assume, for simplicity, that the LO and HI output levels of the transistor-transistor-logic inverters are 0 v and +4 v respectively. Then each of the 16 quantized intervals is 0.25 v wide. Also V_{ref} is set at +2 v. If, for example, 3.4 v (a value within interval 13) is applied to the analog



1. **Nth stage.** In n^{th} stage of successive-approximation a-d converter, an analog input voltage that lies between V_{LO} and V_{HI} is compared with a voltage determined by an average of the reference voltage and weighted values of the more significant bits. Reference voltage Vref is fixed at the midpoint of the analog input range.



2. No clock. Comparator C, compares the analog input voltage with Vref. Thrs defines bit 1 and is averaged with Vref to set the switching level for C,. Bit 2 is averaged with both Vref and a weighted value of bit 1, to set the switching level for C3. Bit 4 is obtained similarly. Each output can drive one TTL load. LM339 comparators can sense input voltages down to ground potential, so only a + 5volt supply is needed.

input, bit 1 goes HI (+4 v), and the input to the noninverting terminal of C_2 is therefore the average of 4 v and 2 v, or 3 v. This sets bit 2 HI. When the weighted levels at bit 1, bit 2, and Vref are now combined, the positive C_3 input voltage is 3.5 v. Bit 3 is therefore set LO and is summed along with Vref and bits 1 and 2 to set the plus input of C4 at 3.25 v; thus bit 4 is set Hi. The output of the circuit is therefore 1101, or decimal 13.

The quad LM3339 comparator operates from a single + 5-v supply and has a settling time of 1.3 microseconds per bit. The totem-pole outputs of the TTL inverters supply the resistor networks with well-clamped voltage levels. In addition, the complement of every bit is available from the LM339 open-collector outputs.