BUILD A SYNCHRONOUS DETECTOR FOR AM RADIO

BY DAVE HERSHBERGER, W9GR

Improves frequency response and removes distortion

THERE IS a misconception that AM radio is inherently a low-fidelity medium. Many people assume that since the channel spacing between AM stations is limited to 10 kHz, there must be some legal restriction to 5-kHz audio response. This is not true, since FCC regulations permit full frequency response to 15 kHz (the same as FM) and the FCC frequency allocation structure takes this into account. However, geographically adjacent transmitters must be spaced at least three 10-kHz channels apart to provide sideband interference protection (FCC Part 73.40, par. A, sub. 12 and 73.182).

AM has a major advantage over FM radio in that it provides better reception in moving vehicles because of the absence of rapid-flutter multipath effects. And AM signals travel much farther than FM signals, thus expanding the listening range.

Most AM radios still use envelope (diode) detection that, when coupled with narrow i-f filtering, greatly restricts the audio bandwidth to produce "muddy" sounding audio because the higher audio frequencies are removed. Envelope detection also produces distortion, further adding to the poor sound.

An advanced method of demodulating an AM signal is to use a wideband i-f (when reception conditions permit), and replace the envelope detector with a synchronous detector. The wide i-f allows a better frequency response, while the synchronous detector will remove distortion produced by selective fading, slight receiver mistuning, modulation overshoots in the i-f filters (transient intermodulation distortion), co-channel interference, and interference or cross modulation. Impulse noise interference is also reduced.

This article will show you how to build a synchronous detector to replace the envelope detector in your AM receiver. It can be used with most any AM (or shortwave) receiver having a 455-kHz i-f. The circuit includes optional SSB detection capability to reject interference such as adjacent channel or other carriers, which occurs primarily in one sideband of a conventional DSB AM signal. When used with a wideband AM tuner, the synchronous detector will offer reception quality rivaling FM.

Theory. A synchronous detector recovers an *unmodulated* carrier from the incoming signal and uses it as a reference to discriminate against noise and distortion. Usually, a phase-locked loop (PLL) is used to regenerate the carrier, which then drives a product detector (multiplier or switch) to recover the modulation. In a more familiar application, synchronous detection is commonly used to demodulate FM stereo L-R and color-TV chrominance signals. Figure 1 shows basic synchronous and envelope detection systems.

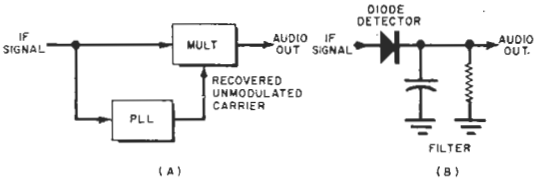
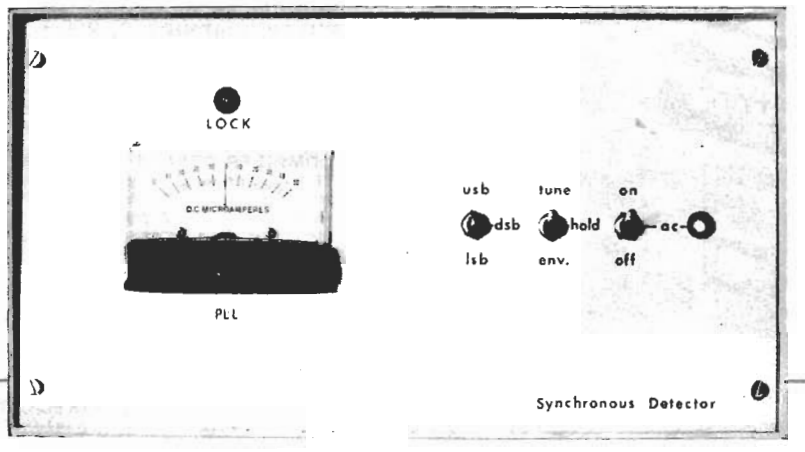


Fig. 1. Simplified diagram of the basic synchronous (A) and envelope (B) detection circuits.

Some examples of common AM phenomena are shown in Fig. 2, along with the resulting outputs of envelope and synchronous detectors. In each case, the synchronous detector gives an undistorted output, as opposed to the envelope detector. (The frequency response may not be flat, but there will be no distortion.) The envelope detector works correctly only when the carrier is large enough, and when the sidebands are perfect mirror images of each other in both amplitude and phase. The synchronous detector, not having this restriction, can demodulate a much wider range of AM signals such as DSB AM, DSB AM with reduced carrier, SSB with full or reduced carrier, vestigial sideband (VSB) AM, quadrature AM,



etc. These forms of AM, which envelope detectors cannot properly demodulate, are produced under commonly occurring natural circumstances. Even though the broadcast signal starts out as conventional DSB AM, receiver mistuning, skywave reflections, etc., can change the AM signal into one or a combination of these other forms.

Circuit Description. The block diagram of a synchronous detector appears in Fig. 3. The circuit accepts a sample of the receiver's i-f (preferably taken from the last i-f stage) and a PLL is used to recover the unmodulated carrier. The circuit also provides automatic switching between envelope and synchronous detection. When the PLL is unlocked during tuning or absence of signal, the envelope detector portion provides the audio output. When the PLL locks onto the carrier, the circuit automatically switches the audio output to the synchronous detector. This action avoids audio-disturbing beat notes that would otherwise occur during tuning.

The circuit in Fig. 3 includes an optional SSB detection feature (shown within the dotted box). With the addition of audio phase-shift networks, it is possible with synchronous detection to receive SSB, or just one sideband of a DSB signal. This technique is usually used as a SSB *generation* method, but works equally well for reception. The circuit also includes a notch filter to remove any audible 10-kHz beats produced by adjacent channel transmitters. The complete schematic is shown in Fig. 4.

Emitter follower *Q1* buffers the i-f input and drives high-speed operational amplifier *IC1*. Automatic gain control (agc) of *IC1* is accomplished by LED-LDR (light-dependent resistor) combination *LDR1*, which produces far less distortion than conventional gain control techniques.

AGC/buffer amplifier *IC1* drives three analog multiplexers (*IC4A*, *IC4B*, and *IC4C*) used as balanced demodulators. The three demodulators, after RC lowpass filtering, provide in-phase ("I"), quadrature ("Q"), and envelope audio. The I channel is the synchronously detected DSB signal, while the Q channel is related to sideband asymmetry. Normally, the Q channel is zero, but if there is phase or amplitude imbalance between the upper and lower sidebands, the Q channel will contain audio. After the PLL locks, the Q channel detector detects phase.

The envelope detector uses differential pair *Q2/Q3* to hard-limit the i-f signal, and the resulting CMOS level square wave drives envelope demodulator *IC2C*. This gets around the limitations of conventional diode detectors, namely, diagonal clipping and diode-threshold distortion. The envelope detector supplies the audio output when the PLL is unlocked, and provides AGC sensing voltage to *IC5A*. The difference between synchronous detector *IC2A* and envelope detector *IC2C* is in the drive signals to the analog multiplexers. The synchronous detector always has a pure unmodulated carrier as its drive signal, while the envelope detector will have phase modulation of its drive during any of the nonideal conditions in Fig. 2.

Switch *S1* in the I circuit selects the detection mode with TUNE, the normal position of the switch. This mode provides slow locking and rapid unlocking. In this mode, the output signal is taken from envelope detector *IC4C*. After tuning in a signal, the logic will switch the output to synchronous detection. The locked bandwidth at 25 Hz is too narrow to track the carrier as the receiver tuning knob is being adjusted. Beat notes are avoided by deliberately delaying the output of lock detector *IC4D* for envelope detection while tuning, and synchronous detection after the hand is taken from the tuning knob.

The middle position of switch *S1*, HOLD, provides rapid locking and slow unlocking, and is intended for use with signals that are subject to fading. If the carrier amplitude momentarily drops below the lock threshold, unlocking is delayed several seconds. With the absence of an input error signal, integrator *IC5B* (the PLL loop filter) will hold the afc voltage during fades. This mode cannot be used for receiver tuning, as beat notes would be heard during the unlock delay period. The last position of *S1* selects the ENV detection mode.

The PLL operates in a wideband mode when unlocked, and automatically switches to a narrowband mode when locked. This allows a wide acquisition range, a fast lock time, and a narrow bandwidth—conflicting requirements in a simple PLL. When unlocked, the hard-limited i-f signal from *Q2/Q3* is compared with the vco signal in phase/frequency detector *IC8*. When the loop locks, a dc component (due to the carrier) will appear at the output of I-channel detector *IC4A*. This level will trip lock detector *IC4D*, an op amp used as a comparator. The lock detector switches the audio output, the PLL control loop, and drives indicator LEDs. When locked, the Q-channel detector is used to control the loop instead of phase/frequency detector *IC8*. The locked-loop bandwidth is about 25 Hz; therefore, when the loop is locked, it operates as a very narrow bandwidth filter, recovering the unmodulated carrier, and rejecting the modulation sidebands.

The vco uses analog multiplexer *IC3C* as the active element. At first this may seem a bit strange, but *IC3C* is connected as a CMOS logic inverter, and is used as such in a conventional CMOS L/C oscillator. Varactor diode *D6* tunes the oscillator to 455 ±15 kHz.

In PLL loop filter *IC5B*, dc feedback is entirely through the vco and Q-channel detector (or *IC8* when un-

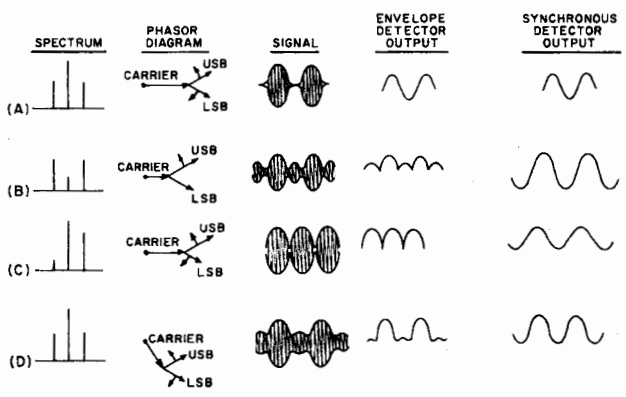


Fig. 2. Some common AM phenomena: (A) Conventional unperturbed AM signal. Both detectors give undistorted outputs. (B) Reduced carrier. Caused by selective fading or directional transmitting antenna. (C) Sideband asymmetry—selective fading or receiver mistuning. (D) Wrong carrier phase—skywave propagation or receiver i-f phase asymmetry.

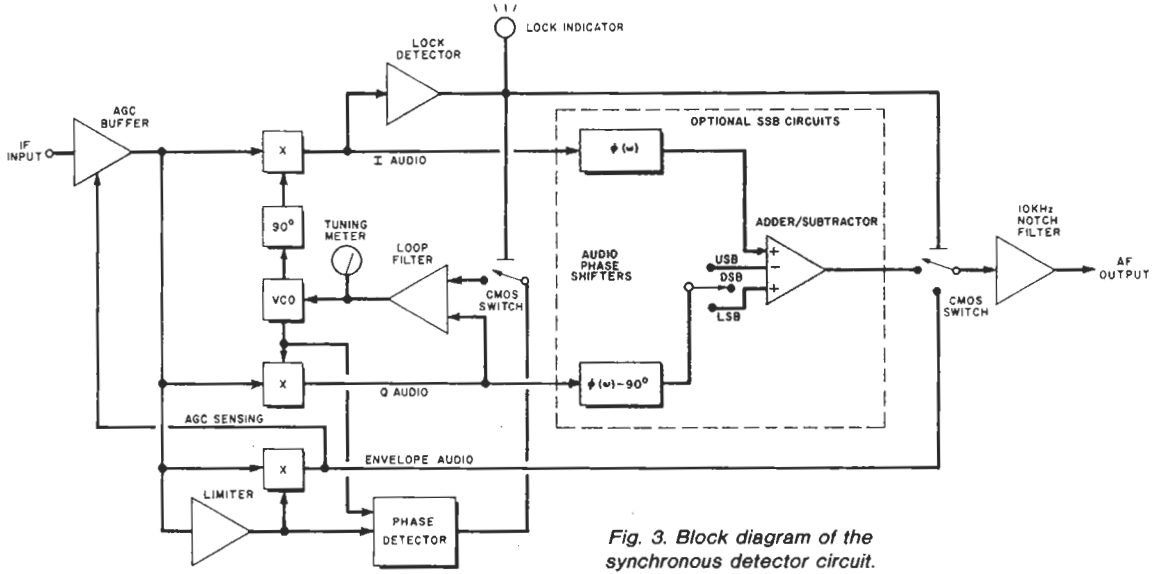


Fig. 3. Block diagram of the synchronous detector circuit.

locked). This forces the Q-channel detector to have a dc component equal to zero, which in turn forces the vco phase to be correct regardless of receiver tuning (Type II loop). Because *IC5B* "sees" varying source resistances as *IC3B* switches, a BiFet or BiMOS type of op amp must be used to minimize bias current effects.

The vco drive to *IC2A*, the I-channel demodulator, must be shifted 90 degrees from the drive to *IC2B*, the Q-channel demodulator. The network comprising *R5*, *L2*, and *C6* forms a passive L/C 90-degree phase shift network.

SSB Option. To obtain SSB reception, the I and Q signals are applied to active audio phase-shift networks having a flat frequency-response charac-

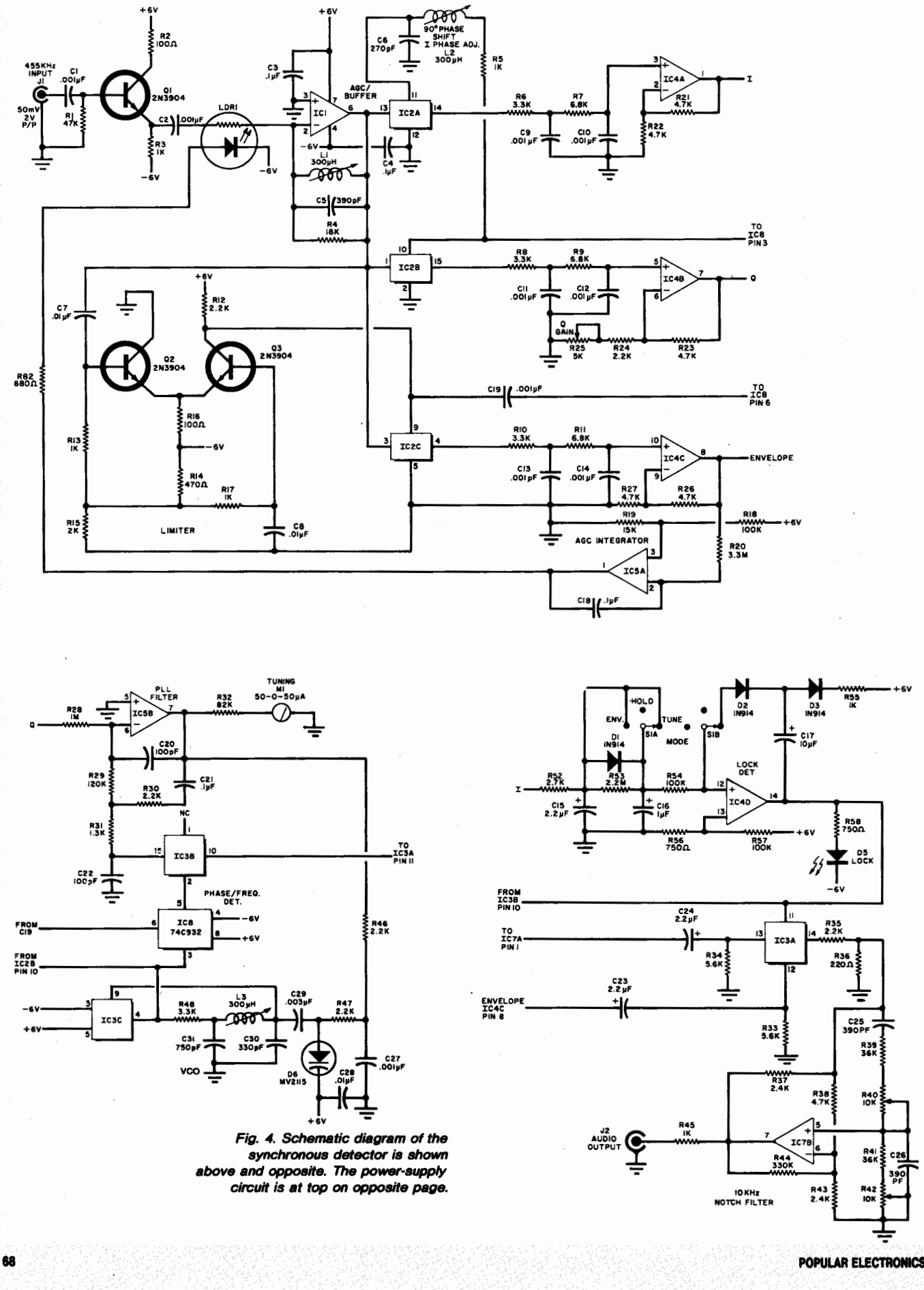
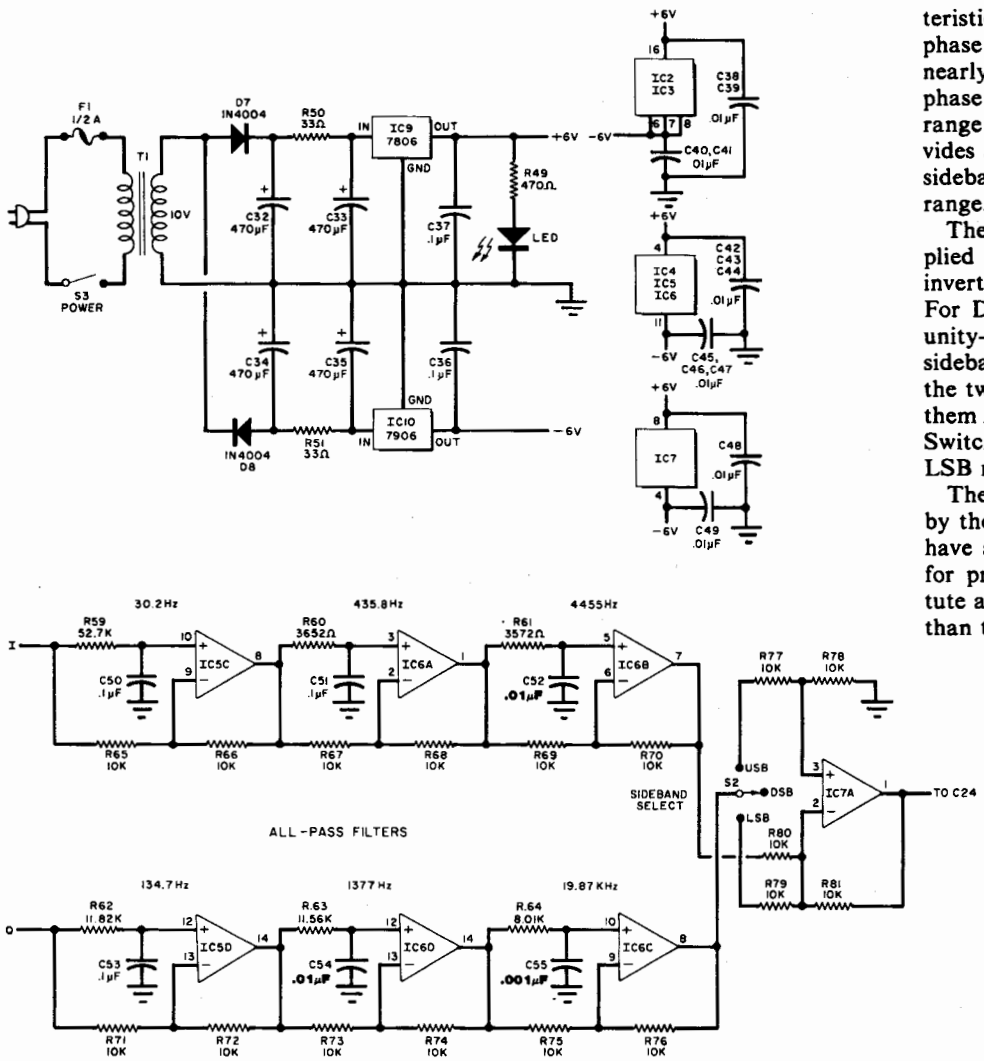


Fig. 4. Schematic diagram of the synchronous detector is shown above and opposite. The power-supply circuit is at top on opposite page.



teristic and a frequency-dependent phase shift. These networks have a nearly constant 90-degree audio phase difference (±3°) over the range of 50 to 12,000 Hz, which provides a minimum of 31-dB unwanted sideband suppression over that range.

The allpass filter outputs are applied to *IC7A*, which is used as an inverting buffer/adder/subtractor. For DSB reception, this IC forms a unity-gain inverting buffer. For lower sideband (LSB) reception, *IC7A* adds the two allpass signals, and subtracts them for upper sideband (USB). Switch *S2* selects the DSB, USB, and LSB modes.

The 10-kHz notch filter is formed by the *IC7B* circuit. This stage must have a high gain/bandwidth product for proper operation. Do not substitute an op amp of lesser performance than the TL072 suggested.

PARTS LIST

C1,C2,C9 through C14,C19,C27—0.001-μF disc capacitor
C3,C4,C36,C37—0.1-μF disc capacitor
C5,C25,C26—390-pF mica capacitor
C6—270-pF mica capacitor
C7,C8,C28,C38 through C49—0.01-μF disc capacitor
C15,C23,C24—2.2-μF, 15-V electrolytic
C16—1-μF, 15-V electrolytic
C17—10-μF, 15-V electrolytic
C18,C21—0.1-μF Mylar capacitor
C20,C22—100-pF disc capacitor
C29—0.003-μF disc capacitor
C30—330-pF mica capacitor
C31—750-pF mica capacitor
C32-C35—470-μF, 25-V electrolytic
C50,C51,C53—0.1-μF, 1% capacitor
C52,C54—0.01-μF, 1% capacitor
C55—.001-μF, 1% capacitor
D1 through D3—IN914 diode
D4,D5—Red LED
D6—MV2115 varactor diode
D7,D8—1N4004 diode
IC1—LM318N op amp
IC2,IC3—CD4053BCN triple two-input CMOS multiplexer
IC4,IC5,IC6—TL074CN quad op amp
IC7—TL072CN dual op amp
IC8—74C932N phase/frequency detector
IC9—7806 or LM340T-6 voltage regulator
IC10—7906 or LM320T-6 voltage regulator
J1,J2—RCA phono jack
L1 through L3—230-440-μH adjustable coil (Midland 25-702, 25-705, or equiv.)
LDR1—LED/LDR (Vactec VTL5C2 or similar)
M1—50-0-50 microammeter (Midland 23-207 or equiv.)
Q1 through Q3—2N3904 transistor
The following are 1/4-W, 10% resistors unless otherwise noted:
R1—47-kΩ
R2,R16—100 Ω
R3,R5,R13,R17,R45,R55—1 kΩ
R4—18 kΩ
R6,R8,R10,R48—3.3 kΩ
R7,R9,R11—6.8 kΩ
R12,R30,R35,R46,R47—2.2 kΩ
R14,R49—470 Ω
R15—2.0 kΩ
R18,R54,R57—100 kΩ
R19—15 kΩ
R20—3.3 MΩ
R21 through R23,R26,R27,R38—4.7 kΩ
R25—5-kΩ potentiometer
R28—1 MΩ
R29—120 kΩ
R31—1.3 kΩ
R32—82 kΩ
R33,R34—5.6 kΩ
R36—220 Ω
R37,R43—2.4 kΩ
R39,R41—36 kΩ
R40,R42—10-kΩ potentiometer
R44—330 kΩ
R50,R51—33 Ω, 1/2 W
R52—2.7 kΩ
R53—2.2 MΩ
R56,R58—750 Ω
R59—52.7 kΩ, 1%
R60—3.65 kΩ, 1%
R61—3.57 kΩ, 1%
R62—11.8 kΩ, 1%
R63—11.6 kΩ, 1%
R64—8.01 kΩ, 1%
R65-R81—10 kΩ, 1%
R82—680 Ω
S1—Dpdt center-off toggle switch
S2—Spdt center-off toggle switch
S3—Spst toggle switch
T1-10 V, 250 mA
Misc.—Prototype board, suitable enclosure, sockets, mounting hardware.

Construction. The synchronous detector can be built using prototyping pc breadboards. While custom pc boards may have a "professional" appearance, users of prototype breadboards enjoy a significant luxury—the ability to modify a circuit without cutting and drilling. If the FCC finally selects an AM stereo system (see POPULAR ELECTRONICS, December, 1978), some may wish to modify this circuit for an AM stereo. The synchronous detector can be changed into an AM stereo decoder for most of the proposed AM stereo systems, with some modifications and additions.

The layout is not very critical as long as good construction practice is observed. Keep large-signal i-f circuits (*Q2, Q3, IC2, IC3,* and *IC8*) away from the i-f input (*Q1, IC1*). Try to keep vco output and limiter output signal leads short.

SSB detection capability is optional. If it is omitted, leave out SSB audio phase shifters *IC5C, IC5D, IC6,* and adder/subtractor *IC7A*. Connect *IC4A* pin 1 to *C23*, and reverse the polarity of *C23*. Replace *R24* and *R25* with a fixed 4.7-kΩ resistor.

Because component tolerances are critical in the allpass (SSB) filters, some selecting and matching of resistors and capacitors is required to obtain the exact RC value in each section. Several methods are available for selecting these components. The easiest way would be to use 1%-tolerance parts. But, since the correct 1%-tolerance parts may be hard to find, there are alternative methods. Resistors *R65* through *R76* must be matched pairs. *R65* must be matched to *R66, R67* matched to *R68*, etc., but each pair need not be matched to any other pair. For example, *R65* and *R66* could both be 10.2 kΩ while *R67* and *R68* could both be 9.7 kΩ. Any value between 1 kΩ and 100 kΩ is suitable for matched pairs *R65-R76*. You can use a digital ohmmeter or bridge to match these parts. Do not use carbon composition resistors because they change value with heat, as during soldering! Carbon-film ("low noise") resistors are recommended for use in the SSB audio phase shifters.

There is an RC pair associated with each noninverting input (for example *R59/C50*). The RC value (ohms, farads) of this pair must satisfy the relation $f_{90} = 1/(2\pi RC)$, where f_{90} is the frequency (in hertz) and the output of a section is shifted 90° in phase from its input. The value of f_{90} for each section is given on the schematic. You can use a digital capacitance meter to measure the capacitors, and a digital ohmmeter to match a series resistor combination to obtain the desired RC product. If you depart from the suggested values on the schematic, keep resistors in the range of 1 kΩ to 100 kΩ, and keep capacitors above 0.001 μF. Do not use ceramic capacitors as they are unstable with temperature.

If accurate resistance and capacitance measuring devices are not available, there is another method, which requires accurate frequency- and voltage-measuring devices, and a sine-wave audio source. The sine-wave generator should have a low output impedance (50 ohms or less). If the generator does not have a low output impedance or if it is unknown, temporarily connect one of the op amp sections as a voltage follower and use it to buffer the output of the signal generator. For each section, temporarily disconnect the inverting input resistor (for example, *R65*) and disconnect the ground lead of the capacitor (for example, *C50*). Apply a sine wave at f_{90} at about 1 volt rms. Make an accurate measurement of the ac signal voltage at the output of the allpass section op amp. Reconnect the capacitor ground lead and adjust the resistor (for example, *R59*) such that the ac voltage at the op amp output drops to 70.71% of its original value. If the initial voltage is 1.000 volt, it should drop to 0.707 volt when the capacitor lead is grounded. After the resistor is adjusted, reconnect the capacitor lead to ground and reconnect the inverting input resistor. Repeat the process for the other five sections.

The PLL dynamics are dependent on the vco sensitivity (output frequency change divided by input voltage change), which, in turn, is dependent on varactor *D6* characteristics. The varactor specified (MV2115) has a capacitance of 100 pF at 4 volts across the diode. If you use this varactor, the vco should tune 455 kHz plus or minus approximately 15 kHz over a −5-to-+5-volt range. The average vco sensitivity is 2.7 kHz per volt. If you use a different varactor, measure the vco frequency versus voltage characteristic and determine the vco sensitivity (kHz/volt), and call this value "X". If X is not 2.7 kHz/volt, multiply the values of the resistances of *R28* and *R31* by X/2.7.

Phase detector *IC8* (74C932) may be hard to obtain. The 74C932 is the phase detector part of the commonly available CD4046 CMOS PLL. The CD4046 may be substituted if the pin connections are rearranged according to the following:

Function	74C932 pin#	CD4046 pin#
V_{DD}	8	16
V_{SS}	4	8
VCO IN	3	3
Limiter In	6	14
Output	5	13
VCO Inhibit (connect to V_{DD})	—	5

All other CD4046 pins remain unconnected.

If the unit specified for *LDR1* cannot be obtained, use a red LED and a cadmium sulphide photocell. Use a photocell having 500 ohms or less resistance at 20 mA of LED current. Then optically seal the pair in a small piece of "heat-shrink" tubing.

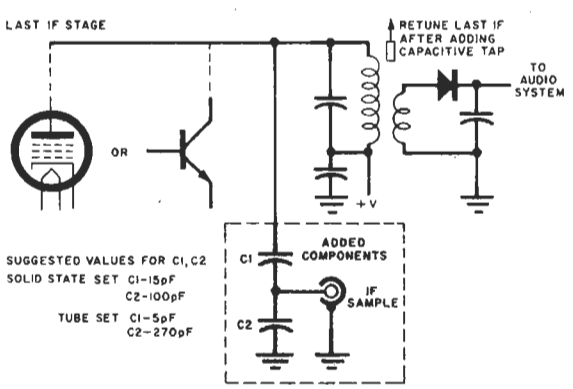


Fig. 5. The signal sample should be taken after the last i-f stage with a capacitive circuit added as shown here.

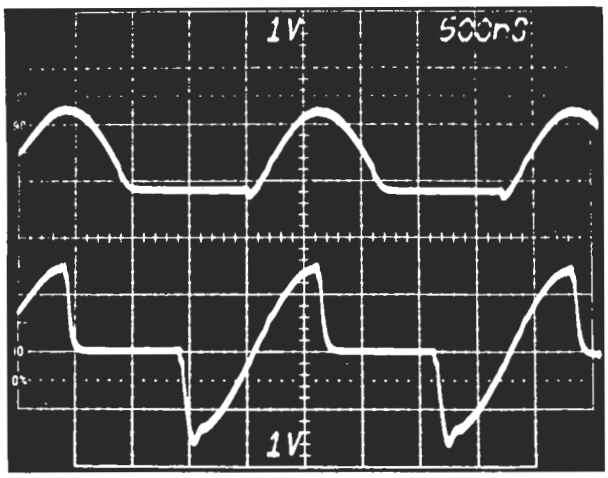


Fig. 6. The I and Q waveforms at pins 14 (top) and 15 (bottom) of IC2.

Receiver Interfacing. Most receivers will work well with the synchronous detector. The only requirement is that the local oscillator (LO) does not have spurious FM modulation. To test for this, tune in the receiver's local oscillator on a general-coverage receiver, using the bfo. If a general-coverage receiver is not available, use a second AM radio for this test, using a broadcast signal above 1MHz as the "bfo." The audio note should be pure, without warbling sounds or pitch variations which indicate spurious FM. If you hear 60-Hz or 120-Hz FM, try improving the receiver power-supply filtering. If you are using a tube-type receiver and notice 60-Hz FM, replace the LO/converter tube. Some tubes may have some heater-to-cathode coupling that, while not affecting normal operation, will introduce a 60-Hz FM component in the LO signal.

The synchronous detector requires an input signal between 50 mV and 2 volts p-p unmodulated carrier. The agc circuit in the detector will establish the correct operating level as long as the input signal is in this range. The input impedance of the synchronous detector is high enough (about 25 kΩ) that it will not disturb most circuits.

The signal sample for the synchronous detector should be taken from the host receiver after all i-f filtering and agc, which usually means at the i-f strip output. In most receivers, a capacitive tap across the primary of the last i-f stage works well, as shown in Fig. 5. The slight additional capacitance introduced by the divider may necessitate realignment of the last i-f transformer. If signal levels are too low for capacitive dividers, try connecting the synchronous detector input directly to the collector of the last i-f stage. Again, it may be necessary to retune the last i-f stage transformer if it exists. If you intend to use your receiver's audio amplifier with the synchronous detector, disconnect the volume control from the envelope detector. Do not disable the envelope detector entirely, as it usually provides agc. Route the audio signal from the synchronous detector back into the volume control, or into an external amplifier.

If your receiver is ac-operated and has no power transformer, be sure to *use an isolation transformer to avoid shock hazard.*

Adjustment. After interfacing the receiver to the synchronous detector, place mode switch *S1* in the TUNE position and tune in a station. If the i-f signal level is above the 50 mV p-p minimum, pin 1 of *IC5* should be between −4.5 and +4.5 volts. Tune *L1* for the most negative voltage at this pin. Adjust *L3* until tuning meter *M1* indicates correct center-channel tuning. The PLL should now be locked, and the LOCK LED should illuminate. Adjust *L2* for maximum dc voltage at pin 1 of *IC4*. As there is also audio present at pin 1, use of a conventional mechanical-movement voltmeter (instead of a digital meter) will avoid confusing readings. This is a coarse adjustment of *L2*. The I and Q channel detector waveforms, at pins 14 and 15 of *IC2*, are shown in Fig. 6.

To adjust the SSB detection circuits, tune in a station which has an interfering carrier, or introduce an interfering carrier from a r-f signal generator. Place sideband selector switch (*S2*) in the position (USB or LSB) which most attenuates the interfering carrier. Alternately adjust Q-channel gain *R25* and I-Phase adjust *L2* for maximum interference attenuation.

To align the 10-kHz notch filter, tune in a station having an adjacent channel interference (10-kHz beat note). If the selectivity of your receiver is too narrow, you will not be able to detect 10 kHz and the notch filter will be unnecessary. But if your receiver does have sufficient bandwidth, alternately adjust *R40* and *R42* for maximum rejection of the 10-kHz beat note.

Operation. In normal operation, SIDEBAND SELECTOR switch *S2* should be set to DSB and MODE switch *S1* to TUNE. Tune the radio as you normally would, but with the aid of tuning meter *M1*. Keep in mind that when the receiver is being tuned, envelope detection is selected, and the LOCK LED will be dark. If the station is fading badly enough that the LOCK LED occasionally goes out, set the MODE switch to the HOLD position. The PLL will then track the received signal through deep fades. The ENV position of the MODE switch selects envelope detection, which can be used for comparison with synchronous detection.

When adjacent channel interference, TV receiver horizontal sweep harmonics, interfering carriers, etc., are present, selection of the USB or LSB mode may provide a significant reduction of the interference, since these types of interference usually affect only one sideband of the AM signal. By receiving the unaffected sideband, an otherwise unlistenable signal can be made usable. For interference which affects both sidebands equally, such as atmospheric or impulse noise, DSB reception is best. (SSB reception rejects half the power of a DSB signal.)

The SSB modes can also provide improved frequency response on narrowband receivers. By tuning off to one side of the station and selecting the appropriate sideband, the frequency response can be significantly improved. (Although detuning can improve frequency response of conventional radios, it will also introduce large amounts of distortion because of envelope detection. Synchronous detection eliminates the distortion caused by detuning.) ◇